

**WHAT IS CLAIMED IS:**

1           1.     A method of fabricating a semiconductor transistor,  
2 comprising:  
3           forming a gate pattern on a semiconductor substrate;  
4           forming a first insulating layer on an entire surface of the  
5 substrate including the gate pattern;  
6           forming L-shaped third and second spacers which are  
7 sequentially stacked on the first insulating layer on a sidewall of  
8 the gate pattern, the third and second spacers each having a  
9 horizontal protruding portion;  
10          simultaneously forming high- and medium-concentration  
11 junction areas in the substrate beyond the L-shaped second  
12 spacer and in the substrate under the horizontal protruding portion  
13 of the L-shaped second spacer, respectively, by performing a high-  
14 concentration ion implantation process using the L-shaped second  
15 spacer and the gate pattern as an ion implantation mask;  
16          annealing the substrate having undergone the high-  
17 concentration ion implantation process;  
18          removing the L-shaped second spacer; and  
19          forming a low-concentration junction area under the  
20 horizontal protruding portion of the L-shaped third spacer by  
21 performing a low-concentration ion implantation process using the  
22 L-shaped third spacer and the gate pattern as an ion implantation  
23 mask.

1           2.     The method as claimed in claim 1, wherein forming the  
2     L-shaped third and second spacers comprises:

3           forming second, third, and fourth insulating layers which are  
4     sequentially stacked on the first insulating layer;

5           anisotropically etching the fourth insulating layer to form a  
6     first spacer on the sidewall of the third insulating layer;

7           etching the third insulating layer, using the first spacer as an  
8     etch mask, to form an L-shaped second spacer having a horizontal  
9     protruding portion under the first spacer; and

10          etching the second insulating layer at the same time as  
11     removing the first spacer to form an L-shaped third spacer having  
12     a horizontal protruding portion under the L-shaped second spacer.

1           3.     The method as claimed in claim 1, wherein the first  
2     insulating layer is made of silicon oxide.

1           4.     The method as claimed in claim 2, wherein the second  
2     insulating layer is made of material having an etch selectivity with  
3     respect to the first insulating layer.

1           5.     The method as claimed in claim 2, wherein the third  
2     insulating layer is made of material having an etch selectivity with  
3     respect to the second insulating layer.

1           6.     The method as claimed in claim 2, wherein the fourth  
2     insulating layer is made of material having an etch selectivity with  
3     respect to the third insulating layer.

1           7.     The method as claimed in claim 2, wherein removing  
2     the first spacer uses an isotropic etch technique.

1           8.     The method as claimed in claim 1, wherein removing  
2     the L-shaped second spacer uses an isotropic etch technique.

1           9.     The method as claimed in claim 1, wherein removing  
2     the L-shaped second spacer includes etching the first insulating  
3     layer exposed on the gate pattern and beyond the L-shaped third  
4     spacer to expose a top surface of the gate pattern and to form an  
5     L-shaped fourth spacer having a horizontal protruding portion  
6     under the L-shaped third spacer.

1           10.    The method as claimed in claim 9, further comprising  
2     forming a silicide layer on the substrate at both sides of the L-  
3     shaped fourth spacer and on the gate pattern, after the low-  
4     concentration ion implantation process is performed.

1           11. The method as claimed in claim 1, wherein the  
2 annealing process step is a rapid thermal process (RTP).

1           12. The method as claimed in claim 1, wherein forming the  
2 medium- and high-concentration junction areas causes the  
3 medium-concentration junction area to have a lower impurity  
4 concentration than the high-concentration junction area, using the  
5 protruding portions of the L-shaped second and third spacers and  
6 the first insulating layer as an ion channeling barrier layer.

1           13. A semiconductor transistor comprising:  
2 a gate pattern formed on a semiconductor substrate;  
3 an L-shaped third spacer having a horizontal protruding  
4 portion, the third spacer being formed on a sidewall surface of the  
5 gate pattern;  
6 an L-shaped fourth spacer having a vertical sidewall  
7 between a vertical sidewall of the L-shaped third spacer and the  
8 gate pattern and a horizontal protruding portion between the  
9 protruding portion of the L-shaped third spacer and the substrate;  
10 a high-concentration junction area formed in the substrate  
11 beyond the L-shaped third spacer;  
12 a low-concentration junction area formed in the substrate  
13 under the horizontal protruding portion of the L-shaped third  
14 spacer; and

15                   a medium-concentration junction area positioned between  
16                   the high- and low-concentration junction areas.

1                   14.    The semiconductor transistor as claimed in claim 13,  
2                   wherein the medium- and low-concentration junction areas are  
3                   formed under the protruding portion of the L-shaped third spacer.

1                   15.    The semiconductor transistor as claimed in claim 13,  
2                   wherein the L-shaped fourth spacer is made of silicon oxide.

1                   16.    The semiconductor transistor as claimed in claim 13,  
2                   wherein the L-shaped third spacer is made of material having an  
3                   etch selectivity with respect to the L-shaped fourth spacer.

1                   17.    The method as claimed in claim 9, wherein the L-  
2                   shaped third spacer is removed before the low-concentration ion-  
3                   implantation process is performed.

1                   18.    The method as claimed in claim 1, wherein a silicon  
2                   oxide layer is formed on the substrate before the low concentration  
3                   ion-implantation process.

1            19.    The method as claimed in claim 4, wherein the second  
2            insulating layer is made of a material selected from the group  
3            consisting of silicon nitride and silicon oxynitride.

1            20.    The method as claimed in claim 4, wherein the third  
2            insulating layer is made of silicon oxide.

1            21.    The method as claimed in claim 6, wherein the fourth  
2            insulating layer is made of a material selected from the group  
3            consisting of silicon nitride and silicon oxynitride.

1            22.    The method as claimed in claim 1, wherein the first  
2            insulating layer is formed to a thickness of between about 2 nm –  
3            5 nm.

1            23.    The method as claimed in claim 2, wherein the sum of  
2            the thickness of the first and second insulating layers is between  
3            about 5 nm - 20 nm.

1            24.    The method as claimed in claim 2, wherein the third  
2            insulating layer is formed to a thickness of between about 20 nm -  
3            70 nm.

- 1            25.    The method as claimed in claim 2, wherein the fourth
- 2            insulating layer is formed to a thickness of between about 30 nm -
- 3            90 nm.